REMARKS

This application has been carefully reviewed in light of the Office Action dated October 17, 2005. Reconsideration and favorable action in this case are respectfully requested.

Applicants note with appreciation that the Examiner has allowed claims 8-11 and claims 2-6, 12-13 and 15-16 would be allowable if rewritten in independent form and if the double patenting rejections were overcome.

The Examiner has objected to claims 1-7 and 12-16 as not being described in the specification at the time the application was filed. Applicants disagree.

The Examiner has rejected claims 1-7 and 12-16 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-19 U.S. Pat. No. 6,684,280 to Chauvel et al (hereinafter the '280 patent), in view of U.S. Pat. No. 6,430,640 Lim (hereinafter the Lim patent). Applicants have reviewed these references in detail and do not believe that they disclose or make obvious the invention as claimed.

The Examiner has rejected claims 1 and 7 under 35 U.S.C. §102(e) as being unpatentable over U.S. Pat. No. 6,430,640 to Lim. Applicants have reviewed this reference in detail and do not believe that it discloses or makes obvious the invention as claimed.

The Examiner has rejected claim 14 under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 6,430,640 to Lim in view of U.S. Pat. No. 5,263,163 to Holt. Applicants have reviewed these references in detail and do not believe that they disclose or make obvious the invention as claimed.

With regard to the objections by the Examiner, having two priority values in a single request and using the higher of the two priority values to arbitrate access to the shared device by using the high or the two priority values in a single access request is clearly disclosed in paragraphs [62] through [64] of the present specification. Specifically, paragraph [63] states:

> When processor 740(0) makes an access request to shared memory 750, a pair of priority values are conveyed to traffic manager arbitration circuitry 1430 along with the request. The first value is the task based priority value provided by task priority register 1410, as discussed earlier. The second value is an address space priority value provided by attribute subfield 309a from TLB 700(0) in response to the address of the access request provided by the processor to the TLB on address bus 742(0). Arbitration circuitry 1430 evaluates both priority values of the pair and compares them to other priority value pairs from other pending requesters, such as processor 740(n). The request having the highest priority value is scheduled to have first access to shared resource 750.

Paragraph [66], describing the specific embodiment of Figure 9, states that "[a] comparison circuit within each processor(n) compares both the task based priority value provided by a register within the processor and an address space priority value provided by the TLB associated with the processor and provides the highest priority value on priority signals 1209(n)."

If the Examiner does not believe that these passages show every element of the claims, Applicants request that he call their attorney, Alan Lintel, to discuss the situation.

With regard to the double patenting rejection, Applicants believe that this rejection has no merit whatsoever. The '280 patent teaches the association of *one and only one* priority value with a memory access request. The Examiner's apparent position that claim 17 specifies a priority value and claim 18 specifies a priority value and, *abracadbra*, we suddenly have a hybrid claim combining the two which recites two priority values is simply not credible. Claim 17 does not claim a memory access with two

priority values. The pertinent elements of claim 17 are "providing *a* respective access priority value with each of the plurality of access requests that is responsive to the respective software priority state of the respective program module; and arbitrating for access to the shared resource by using the ***respective*** access priority values provided with the plurality of access requests." The claim is explicit – each memory access has one priority value, each arbitration uses the one priority from each competing memory access.

Claim 18 of the '280 patent does not add another priority value to the memory access. Claim 18 specifies that if the program module is a task, then the software priority state of the program module is set according to the task priority. There is no teaching, or claiming, of a memory access associated with a task priority *and* a software priority. The software priority is simply set according to the task priority. The memory access still has only *one* priority state associated with it.

With respect to the rest of the analysis of the double patenting rejection, the Examiner is requested to refer to Applicants' previous responses. In summary, the claims of the '280 patent recite only a single comparable element to the independent claims of the present case, namely "initiating an access request by each of the plurality of devices". In every other element, the '280 patent fails to show two priority values per memory access or the use of the higher priority value of each request to arbitrate memory access requests.

Lim does not correct the deficiency in the '280 patent. The disclosure at column 14, line 11 clearly refers to comparing *single* priority values per access request, *each from a different device*. This is abundantly clear from the immediately preceding sentence – "the arbitration unit 404 for each entity 400 wishing to access shared resource 408 provides *a* priority value 410 for comparison." (column 14, lines 7-10). The second passage cited by the Examiner describes using a processor ID to *break ties* when the priority value is the same for two competing requests. The only embodiment described in

Lim appends the processor ID to the least significant bits of the priority value such that two priorities cannot be equal. This would comprise a single priority value for a memory access. Nonetheless, *even if the processor ID was considered to be a separate priority value*, it does not show the present invention as claimed. In each of claims 1 and 7, the *higher* of two priority values provided in a single access request is used for arbitration – this is much different than providing a second priority value that is used to break ties and provides significantly different results. In Lim, a higher priority value for a first task would *always, without exception* take precedence over a second task with a lower priority value *no matter what value was assigned to the processor ID associated with the second task.*

Additionally, Claim 7 specifies that the two separate priority values are *variable*; there is no showing in Lim that the processor ID is variable.

The examples cited by the Examiner (paragraphs [30]-[34] of the present application) are directed to a different embodiment. The embodiment being claimed in the application is described primarily in paragraphs [62]-[68] of the application.

An example of the different results attributable to the present invention are shown in the table below. In this example, a lower number is a higher priority.

Processor 1 Task priority	Processor 1 address page priority	Processor 2 Task priority	Processor 2 address page priority	Arbitration Result
5	15	20	0	Processor 2 (address priority)
5	15	0	20	Processor 2 (address priority)
5	15	10	20	Processor 1 (task priority)

As can be seen from the example above, neither the task priority nor the address page priority acts as a tie-breaker; instead, either priority can be determinative of the result of the arbitration based on its relative priority value. This allows a lower priority task to have higher access priority if it is addressing a page of memory which is considered extremely important; similarly, it allows a task that has a very high priority value to have priority regardless of what page is accessed. This can be an extremely powerful manner of arbitrating memory accesses which simply can not be accomplished by the prior art.

With regard to the 102(e) rejection over Lim, the same arguments apply. Lim shows a single priority value; there is no indication in Lim that the processor ID is anymore than a tie-breaker and there is no teaching that the processor ID has any priority function. Second, *even if the processor ID in Lim was interpreted to be a second priority* value provided with a request, claims 1 and 7 specifically state that arbitration is performed using the *higher* or the two priority values provided with an access request to a shared resource – there is no such teaching in Lim, nor would it make any sense, to use the *processor ID* associated with an access request as the *primary* priority value (as opposed to a tie-breaker) if the processor ID was of higher value than the actual priority value associated with the access request. Third, claim 7 specifically states that each of the two priority values associated with an access request are *variable*, and there is no indication in Lim that the processor ID is variable. Fourth, the Examiner already has stated that Lim does not show two priority values with an access request on multiple occasions.

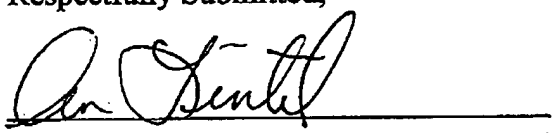
With regard to the 103(a) rejection of claim 14, Applicants believe that since this claim is dependent upon claim 1, it is novel over the Lim and Holt references. Applicants do not believe that Holt shoes an address space priority value. It is clear from the passage cited by the Examiner that the address bits are separate from the priority bits, and there is not priority value that is responsive to the address specified by the request.

The Commissioner is hereby authorized to charge any fees or credit any overpayment, including extension fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Alan W. Lintel, Applicants' Attorney at (972) 664-9595 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



Alan W. Lintel
Attorney for Applicant(s)
Reg. No. 32478

December 19, 2005
Anderson, Levine & Lintel
14785 Preston Rd.
Suite 650
Dallas, Texas 75254
Tel. (972) 664-9595